PVP 14

Code: EC6T1

III B.Tech-II Semester–Regular/Supplementary Examinations–March 2019

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) What is Latch – up in CMOS circuits?
b) What is body effect? Which parameters are responsible for it?
c) Draw a stick diagram of CMOS inverter.
d) Define a buried contact and a butting contact of MOSFET.
e) What is floor planning and placement in VLSI circuits?
f) Distinguish pass transistor logic and Transmission gate logic.
g) What is the difference between PLA and PAL?
h) What is an ASIC? List out different types of ASICs.
i) What is the difference between exhaustive and random test approaches?
j) Write about stuck open and short faults.
k) Draw the Layout encodings for NMOS and PMOS transistors.

PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Derive the expression for Drain to Source current in both Saturated and Non- saturated regions of MOS transistor. 8 M

b) Explain the operation of enhancement mode MOSFET with neat diagrams. 8 M

3. a) Define standard unit of capacitance and calculate $\square C_g$ for 5 μm MOS circuits. 8 M

b) Discuss briefly the λ – based design rules for layers, wires and transistors. 8 M

4. a) What are the limitations of Scaling. Derive the scaling factors for any two device parameters. 8 M

b) Design a transmission gate based inverter logic and explain. 8 M

5. a) Discuss the differences between FPGAs and CPLDs. 8 M

b) Design a Half-adder logic using programmable logic arrays. 8 M

6. a) What is the need for testing? Discuss different types of testing. 8 M

b) Discuss scan based techniques of testing a design. 8 M